REMARKS

With this Response, claims 1-2, 11-12, and 20-21 are amended. Claims 44-50 are added. Therefore, claims 1-50 are pending.

Allowable Subject Matter

Applicants note that claims 3, 13, and 22 were objected to as dependent upon rejected independent base claims. Applicants respectfully submit that the rejection of the base claims is overcome herein; therefore, these claims are allowable as written. Therefore, Applicants respectfully request that the objection to these claims be withdrawn.

Claim Rejections - 35 U.S.C. § 102

Claims 1-2, 4-12, 14-21, and 23-41 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2001/0052054 A1 of Franke et al. (*Franke*). Applicants respectfully submit that rejection of these claims under the cited reference is improper because the cited reference fails to disclose every limitation of the claims as required by MPEP 2131.

Claim 1 recites the following:

> initializing a circuit said circuit having at least one memory element coupled to a memory bus on a host system;
> **monitoring signals on the memory bus;**
> detecting a first sequence of signals, the first sequence of signals including a reserved memory address; and
> **switching control** of the at least one memory element to the circuit in response to detection of the reserved memory address.

Independent claims 11, 20, and 36 similarly recite monitoring signals on a memory bus and switching control of a memory in response to detecting a reserved memory address.

The Final Office Action newly cites *Franke* as disclosing the invention as claimed. Specifically, the Office Action at page 2 asserts each of *Franke*'s processors with associated

caches (references 101 and 102, respectively) in Figure 1 disclose circuits with memory elements monitoring signals on a memory bus. In contrast to what is asserted in the Office Action, Applicants note that references 101 and 102 of Figure 1 of *Franke* are only discussed as coupled to, and monitoring signals on System Bus 100. The System Bus 100 is described in *Franke* as "a system communications bus," (paragraphs [0032], [0046]) and a "typical communications bus" (paragraph [0038]), and no suggestion is given in *Franke* that the system bus is a memory bus. Applicants also note that System Bus 100 is coupled to various I/O Controllers 104, which may not normally be considered elements that would have access to a memory bus. Thus, Applicants contend that *Franke*'s processors at most could be understood to monitor signals on a system communication bus, and not on a memory bus, as recited in the claims. Because *Franke* fails to disclose or suggest monitoring signals on a memory bus, *Franke* fails to disclose every element of the claims, and thus fails to provide support for a prima facie case of anticipation under MPEP §2131. Therefore, the cited reference fails to support an anticipation rejection of claims 1, 11, 20, and 36.

Furthermore, even assuming the system bus of *Franke* could be interpreted as a memory bus as recited in the claims, which Applicants submit would be an improper interpretation, *Franke* fails to disclose or suggest switching control of a memory, as recited in the claims. The Office Action at page 3 asserts: "when an address assigned to one of the processors is detected, control of the memory element is switched to the processor assigned to have access to the memory region containing the assigned address." Applicants respectfully submit that the reference fails to provide support for this assertion. To the contrary, *Franke* refers to "[snooping] on the communications bus [waiting] for a transaction, either a request or a response issued by one of the processors 101." Importantly, *Franke* specifies that the request is

preliminarily serviced, with the results being placed in a queue as well as delivered to the requesting processor as the validity of the transaction is determined. The results in the queue are discarded if, after the fact, it is determined that the transaction was invalid, and/or the processor that requested the invalid memory location is reset. See, e.g., paragraphs [0047], [0048], [0056]. Noticeably, the requesting processor is **not** blocked access to the memory location, as would be expected if control were to be "switched" to the requesting processor, but the results are simply invalidated, and the requesting processor, which already has obtained the data from the invalid request, is reset to prevent cache incoherency across the system. In all descriptions in *Franke*, arbitration of the system bus is assumed, which provides access to the processor to make the request. *Franke* explains that the reason the transactions are halted to await a validity check is that "[d]ue to the timing constraints on the bus, **nothing can be done to these transactions** [to interfere with them]." Paragraph [0021]. Because of the timing constraints on System Bus 100, the transactions must be allowed to proceed, and *Franke*'s choice of remediation is therefore not denying switching of control, but post-transaction invalidation of obtained data. Thus, the disclosure of *Franke* is contrary to the assertion made in the Office Action.

Therefore, the cited reference fails to disclose or suggest at least one element of the independent claims 1, 11, 20, and 36, and so fails to anticipate the invention as claimed. Furthermore, claims 2-10 and 30-31, 12-19 and 32-33, 21-29 and 34-35, and 37-41, as depending from the independent claims, respectively, necessarily include the limitations of the independent claims. Because the reference fails to set forth every element of the independent claims, the reference necessarily fails to set forth every element of the claims depending from the independent claims. Therefore, Applicants submit that these claims are not anticipated by the cited reference for at least the reasons discussed above with respect to the independent claims.

Claim Rejections - 35 U.S.C. § 103

Claims 42-43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Franke*. Applicants note that this rejection is predicated upon the rejection of claim 36, from which claims 42-43 depend. The Office Action merely further asserts that it is well known in the art to use SDRAM memories and DIMMs. Whether or not it is well known to use SDRAM and DIMMs, Applicants submit that the rejection of claim 36 is improper, as set forth in detail above, and an understanding of SDRAM and DIMMs, whether well known or otherwise, fails to cure the deficiencies of *Franke* as noted above. Thus, Applicants respectfully submit that rejection of these claims is improper under the cited reference for at least the reasons set forth above.

New Claims

Applicants present herein new claims 44-50 for examination. Applicants respectfully submit that these claims include limitations not found in the cited references. Therefore, Applicants respectfully submit that these claims are allowable over the cited art.

Conclusion

For at least the foregoing reasons, Applicants submit that all rejections have been overcome. Therefore, Applicants submit that all pending claims are in condition for allowance and such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
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